AMENDMENTS TO THE SPECIFICATION

Please amend the line in the specification on page 1 immediately before paragraph [0001] as follows:

~~TECHNICAL FIELD~~BACKGROUND OF THE INVENTION

Please add the following line to the specification on page 1 immediately before paragraph [0001]:

1. Field of the Invention

Please amend the line in the specification on page 1 immediately before paragraph [0002] as follows:

~~BACKGROUND ART~~2. Description of the Related Art

Please amend the line in the specification on page 6 immediately before paragraph [0010] as follows:

~~DISCLOSURE~~ SUMMARY OF THE INVENTION

Please amend the line in the specification on page 7 immediately before paragraph [0017] as follows:

~~MEANS FOR SOLVING THE PROBLEM~~

Please insert the following beginning on page 7 of the specification immediately before paragraph [0017]:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is one example of the BDD for CF.

FIG. 2 is the explanation drawings of shorting operation.

FIG. 3 is the structure diagram of logic circuit obtained by decomposing a multiple-output logic function into two.

FIG. 4 is one example of reduction in width by algorithm 1 to BDD_for_CF of the incompletely specified multiple-output function representing the truth table in Table 4.

FIG. 5 is the structure diagram of BDD_for_CF after the deletion by shorting.

FIG. 6 is the truth table and the BDD_for_CF of ADR2.

FIG. 7 is the explanation drawings of the the process that transforms the sub-graph including the root node into an LUT, when the BDD for characteristic function representing ADR2 are partitioned into two.

FIG. 8 is the explanation drawings of deletion by shorting of BDD_for_CF of ADR2 and transformation process into LUT.

FIG. 9 is the explanation drawings of deletion by shorting of BDD_for_CF of ADR2 and transformation process into LUT.

FIG. 10 is the structure diagram of the "Device for Logic Synthesis" and the peripheral equipment according to Embodiment 1 of the present invention.

FIG. 11 is the flowchart showing the whole flow of the method for logic synthesis according to Embodiment 1.

FIG. 12 is the flowchart representing the decision process of the variable orderings.

FIG. 13 is the data structure diagram of the node table.

FIG. 14 is the reduced BDD_for_CF of the multiple-output logic function f(X) in Eq. (31) and the node table corresponding to the BDD_for_CF.

FIG. 15 is the BDD_for_CF of the multiple-output logic function f(X) in Eq. (31) and the node table corresponding to the BDD_for_CF.

FIG. 16 is the flowchart representing the synthesis process of the LUT cascade logic circuit.

FIG. 17 is the experimental results of the synthesis of LUT cascades using the logic synthesis method of the present invention.

FIG. 18 is the structure diagram of a "Device for Logic Synthesis" and its peripheral device of Embodiment 2 with respect to present invention.

FIG. 19 is the structure diagram of the "Device for Reducing the Width of Graph" 20 in FIG. 18.

FIG. 20 is a flowchart representing the whole flow of the graph width reduction process of the "Device for Reducing the Width of Graph" 20.

FIG. 21 is a flowchart representing the flow of the node covering process of the compatible graph by clique set.

FIG. 22 is the explanation drawings of the graph width reduction process of the BDD_for_CF of the incompletely specified function of Example 10.

FIG. 23 is the explanation drawings of the graph width reduction process of the BDD_for_CF of the incompletely specified function of Example 10.

FIG. 24 is the explanation drawings of the graph width reduction process of the BDD for CF of the incompletely specified function of Example 10.

FIG. 25 is the comparative diagram of synthesis results of LUT cascades using the benchmark functions 5-7-11-13 RNS.

EXPLANATION OF REFERENCES

1, 1' "Device for Logic Synthesis"

2 "Means to Store the Logic Specification"

3 input device

4 output device

5 "Means to Decide the Ordering of Output Variables"

6 "Means to Decide the Ordering of All the Variables"

7 "Means to Generate BDDs"

8 "Means to Store Node Table"

9 "Means to Optimize the Ordering of Variables"

10 "Means to Find the Dividing Lines"

11 "Means to Reduce by Shorting"

12 "Means to Measure the Width of BDDs"

13 "Means to Compute the InterMediate Variables"

14 "Means to Generate LUTs"

15 "Means to Re-construct BDDs"

16 "Means to Store LUTs"

20 "Device for Reducing the Width of Graph"

21 "Means to Measure the Height of BDDs"

22 "Means to Find the Dividing Lines"

23 "Means to Generate Column Functions"

24 "Means to Store Column Functions"

25 "Means to Generate Compatible Edges"

26 "Means to Store Compatible Graphs"

27 "Means to Generate Cliques"

28 "Means to Store Clique Data"

29 "Means to Reconstruct Assigned BDD"

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

Please amend the specification beginning on page 44 on the line immediately before paragraph [0130] as follows:

~~BRIEF DESCRIPTION OF THE DRAWINGS~~

~~FIG. 1 is one example of the BDD_for_CF.~~

~~FIG. 2 is the explanation drawings of shorting operation.~~

~~FIG. 3 is the structure diagram of logic circuit obtained by decomposing a multiple-output logic function into two.~~

~~FIG. 4 is one example of reduction in width by algorithm 1 to BDD_for_CF of the incompletely specified multiple-output function representing the truth table in Table 4.~~

~~FIG. 5 is the structure diagram of BDD_for_CF after the deletion by shorting.~~

~~FIG. 6 is the truth table and the BDD_for_CF of ADR2.~~

~~FIG. 7 is the explanation drawings of the the process that transforms the sub-graph including the root node into an LUT, when the BDD for characteristic function representing ADR2 are partitioned into two.~~

~~FIG. 8 is the explanation drawings of deletion by shorting of BDD_for_CF of ADR2 and transformation process into LUT.~~

~~FIG. 9 is the explanation drawings of deletion by shorting of BDD_for_CF of ADR2 and transformation process into LUT.~~

~~FIG. 10 is the structure diagram of the "Device for Logic Synthesis" and the peripheral equipment according to Embodiment 1 of the present invention.~~

~~FIG. 11 is the flowchart showing the whole flow of the method for logic synthesis according to Embodiment 1.~~

~~FIG. 12 is the flowchart representing the decision process of the variable orderings.~~

~~FIG. 13 is the data structure diagram of the node table.~~

~~FIG. 14 is the reduced BDD_for_CF of the multiple-output logic function f(X) in Eq. (31) and the node table corresponding to the BDD_for_CF.~~

~~FIG. 15 is the BDD_for_CF of the multiple-output logic function f(X) in Eq. (31) and the node table corresponding to the BDD_for_CF.~~

~~FIG. 16 is the flowchart representing the synthesis process of the LUT cascade logic circuit.~~

~~FIG. 17 is the experimental results of the synthesis of LUT cascades using the logic synthesis method of the present invention.~~

~~FIG. 18 is the structure diagram of a "Device for Logic Synthesis" and its peripheral device of Embodiment 2 with respect to present invention.~~

~~FIG. 19 is the structure diagram of the "Device for Reducing the Width of Graph" 20 in FIG. 18.~~

~~FIG. 20 is a flowchart representing the whole flow of the graph width reduction process of the "Device for Reducing the Width of Graph" 20.~~

~~FIG. 21 is a flowchart representing the flow of the node covering process of the compatible graph by clique set.~~

~~FIG. 22 is the explanation drawings of the graph width reduction process of the BDD_for_CF of the incompletely specified function of Example 10.~~

~~FIG. 23 is the explanation drawings of the graph width reduction process of the BDD_for_CF of the incompletely specified function of Example 10.~~

~~FIG. 24 is the explanation drawings of the graph width reduction process of the BDD_for_CF of the incompletely specified function of Example 10.~~

~~FIG. 25 is the comparative diagram of synthesis results of LUT cascades using the benchmark functions 5-7-11-13 RNS.~~

~~EXPLANATION OF REFERENCES~~

~~1, 1' "Device for Logic Synthesis"~~

~~2 "Means to Store the Logic Specification"~~

~~3 input device~~

~~4 output device~~

~~5 "Means to Decide the Ordering of Output Variables"~~

~~6 "Means to Decide the Ordering of All the Variables"~~

~~7 "Means to Generate BDDs"~~

~~8 "Means to Store Node Table"~~

~~9 "Means to Optimize the Ordering of Variables"~~

~~10 "Means to Find the Dividing Lines"~~

~~11 "Means to Reduce by Shorting"~~

~~12 "Means to Measure the Width of BDDs"~~

~~13 "Means to Compute the InterMediate Variables"~~

~~14 "Means to Generate LUTs"~~

~~15 "Means to Re-construct BDDs"~~

~~16 "Means to Store LUTs"~~

~~20 "Device for Reducing the Width of Graph"~~

~~21 "Means to Measure the Height of BDDs"~~

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~~23 "Means to Generate Column Functions"~~

~~24 "Means to Store Column Functions"~~

~~25 "Means to Generate Compatible Edges"~~

~~26 "Means to Store Compatible Graphs"~~

~~27 "Means to Generate Cliques"~~

~~28 "Means to Store Clique Data"~~

~~29 "Means to Reconstruct Assigned BDD"~~

~~BEST MODE FOR CARRYING OUT THE INVENTION~~

Please amend paragraph [00132] of the specification on page 46 as follows:

Hereinafter, preferred embodiments of the present invention will be ~~concretely~~ described with reference to the drawings.